7. (Amended) A modelling file stored on a computer readable medium and comprising a first code portion holding a test functions file defining the communication attributes of a processor with a peripheral of an ASP to be simulated and including the state of the test function file after a predetermined simulation phase and a second code portion holding an interface functions file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface functions file after the predetermined simulation phase, wherein the code portions are within a circuit level simulation language and are executable by a computer in which the modelling file is loaded to simulate the ASP at circuit level for a subsequent simulation phase.

REMARKS

In response to the Final Office Action mailed October 22, 2002, and the Office Communication mailed January 30, 2003, Applicant respectfully requests reconsideration.

Claims 1-7 are pending in the application. Claims 1-5 are allowed. Claim 7 has been amended solely for the purposes of clarification, to patentability on the merits. A marked-up version of claim 7 is provided on a separate sheet captioned "MARKED-UP CLAIMS."

The Office Action rejected claims 6 and 7 under 35 U.S.C. §102(e) as being anticipated by Aleksic (U.S. Patent Number 5,995,736). Applicant respectfully traverses this rejection.

Aleksic is directed to a method and system for automatically modeling registers for integrated circuit design. As illustrated in Figure 2 of Aleksic, a system 32 for automatically modeling registers includes a common register description source data 34, which is description data representing grouped register data in the form of a text file. This text file serves as the source for automatically generating hardware design simulation code and behavioral model code (Col. 5, lines 9-18). System 32 also includes a model register generator 36 which accesses the source file 34 to generate the behavioral model code, the hardware simulation code, the application interface layer code 42, automatic register tests 44, integrated circuit documentation 46, software header information 48, and connection templates 49 (Col. 5, lines 19-29). The behavioral model code 40 and the hardware simulation code 38 make up a coded register layer which defines characteristics of each register block. The hardware design simulation code 38

and the behavioral model register code 40 is based on the register specification source data, thus the register layer is also based on the register specification source data 34 (Col. 5, lines 43-54).

Aleksic discloses that the behavioral model register code and the hardware design simulation code are both generated from the register specification source 34. Moreover, Aleksic discloses that the behavioral model code and the hardware simulation code are also tested in parallel. For example, in Col. 7, lines 61 thorough Col. 8, line 7, Aleksic discloses that once the behavioral model register code 40 and the hardware design simulation code are generated, the system complies the code in a form suitable for testing. The automatic register generator 36 pulls register file data from the register specification source 34 to populate test code templates for testing both the behavioral model register code 40 and the hardware design simulation code 38. The system then runs the test on the behavioral model register code and the hardware design code using the register test code 44.

Claim 6 Patentably Distinguishes Over Aleksic

Claim 6 is directed to a computer system for simulating an ASP. The computer system comprises first processor means including execution means for simulating a functional model in a high level language and output means for outputting the state of the functional model at the end of a predetermined simulation phase and means for converting the function model, including its state at the end of the predetermined simulation phase, into a simulation language for simulating the ASP at circuit level.

Aleksic fails to disclose or suggest a system for simulating an ASP in which the state of the functional model at the end of a simulation phase is used to simulate the ASP at the circuit level in a subsequent simulation phase. Aleksic instead discloses generating and testing the behavioral model and the hardware simulation model in parallel. For example, beginning at column 7, line 61 and at box 94 of Figure 5, Aleksic discloses that both the behavioral model register code (used to simulate the behavior of the ASIC in a high level language) and the hardware design simulation code (used to simulate the ASIC at the circuit or gate level) may be compiled into a form suitable for testing and then tested together (i.e., in parallel) using the same register code templates. Nowhere does Aleksic disclose or suggest that the state of the functional

model at the end of a predetermined simulation phase may be converted into a simulation language for simulating the ASP at the circuit level in a subsequent simulation phase.

As described in Applicant's specification at page 14, line 19 – page 15, line 21, the simulation of an ASP at the circuit level is typically very slow. However, it is possible to speed up this simulation by running the functional model for an initialization or set up phase (or any other phase) and, at the end of that phase, extracting the state of the model at a particular point in time and saving it in a modelling file. This file may be translated into a simulation file, which can be loaded into the circuit level simulation process and used in the circuit level simulation process to simulate the ASP at the circuit level in a phase that is subsequent to the phase simulated with the functional model. This extraction of state from the functional model at a particular point in time in order to "kick start" the circuit level model simulations significantly reduces the overall simulation time. Accordingly, because Aleksic does not disclose or suggest this aspect of Applicant's claimed invention, claim 6 patentably distinguishes over Aleksic and it is respectfully requested that the rejection of claim 6 under 35 U.S.C. §102(e) be withdrawn.

Claim 7 Patentably Distinguishes Over Aleksic

Claim 7 is directed to a modelling file stored on a computer readable medium. The modelling file comprises a first code portion and a second code portion. The first code portion holds a test functions file defining the communication attributes of a processor with a peripheral of an ASP to be simulated and including the state of the test function file after a predetermined simulation phase. The second code portion holds an interface functions file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface functions file after the predetermined simulation phase. The code portions are within a circuit level simulation language and are executable by a computer in which the modelling file is loaded to simulate the ASP at circuit level for a subsequent simulation phase.

As discussed above, Aleksic discloses generating and testing the behavioral model and the hardware's emulation model in parallel. Aleksic fails to disclose or suggest using state information from the simulation of the functional model in one phase as input to circuit level simulation of the hardware model in a subsequent simulation phase. Thus, claim 7 patentably

distinguishes over Aleksic. Accordingly, it is respectfully requested that the rejection of claim 7 under 35 U.S.C. §102(e) be withdrawn.

CONCLUSION

In view of the foregoing remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes after this response that the application is not in condition for allowance, the Examiner is requested to call Applicant's attorney at the number listed below to discuss any outstanding issues relating to allowability.

If this response is not considered timely filed, and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by the enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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MARKED-UP CLAIMS

Claim 7 has been amended as follows:

7. (Amended) A modelling file stored on a computer readable medium and comprising a first code portion holding a test functions file defining the communication attributes of a processor with a peripheral of an ASP to be simulated and including the state of the test function file after a predetermined simulation phase and a second code portion holding an interface functions file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface functions file after [a] the predetermined simulation phase, wherein the code portions are within a circuit level simulation language and are executable by a computer in which the modelling file is loaded to simulate the ASP at circuit level for a subsequent simulation phase.